Experiment 4: Algorithm Experiment

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# Experimental purpose

* + 1. Master the working principle of arithmetic and logical operation units.
    2. Familiar with the circuit composition of simple arithmetic operators.
    3. Familiar with the arithmetic and logic operation functions of the 4-bit operation function generator (74LS181).

# Experimental requirements

* + 1. Prepare for the experiment, understand the circuit diagram, and be familiar with the functions and connection methods of each pin of the chip used in the experiment.
    2. Complete the experiment carefully and conscientiously according to the requirements of the experimental content and steps.
    3. Write an experimental report.

# Experimental circuit

The main digital functional devices used in this experiment include a 4-bit arithmetic logic operation unit 74LS181, an 8-bit data latch 74LS273, an 8-group bus transceiver 74LS245 with three state output, single pulse, switch, data display light, etc. Please refer to the chip data manual for detailed instructions on the chip.

Figure 2.1 shows the circuit diagram of the arithmetic unit used in this experiment. The bold marked lines at the tail of the figure represent the control signal lines, while the rest represent the data lines. The control signals involved in the experimental circuit are as follows:

* + 1. M: Select the operation mode of ALU (M=0, arithmetic operation; M=1, logical operation).
    2. S3, S2, S1, S0: Select the operation type of ALU, for example, if set to 1001 in arithmetic operation mode, ALU Perform addition operations, see 74LS181 menu 3-1 for details.
    3. Cn: The carry signal input to the lowest bit of ALU, with carry input when Cn=0 and no carry input when Cn=1.
    4. Cn+4: The carry signal output from the highest bit of the ALU. When it is 0, there is a carry output, and when it is 1, there is no carry output.
    5. P1: Pulse signal, input data into DR1 on the rising edge. The 74LS273 trigger does not affect the output when the clock input is at a high or low level. Only at the rising edge of the clock pulse will the input data be sent to the output and locked.
    6. P2: Pulse signal, input data into DR2 at the rising edge.
    7. MR: The reset signal of chip 74LS273 is effective at low levels. When MR is level, the data output pin of 74LS273 is set to zero.
    8. ALU-BUS: The ALU outputs a three state gate enable signal. When it is 0, the value of the 74LS245 input pin is output from the output pin, thereby outputting the ALU operation result to the data bus.
    9. SW BUS: The switch outputs a three state gate enable signal, and when it is 0, sends SW7~SW0 data to the data bus.

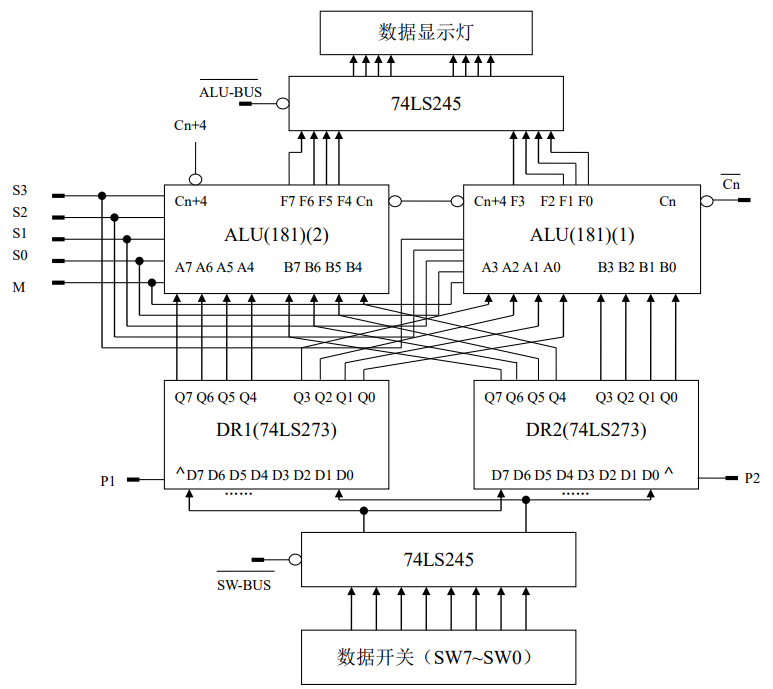


Figure 2.1 Experimental circuit of arithmetic unit

# Experiment Principles

The experimental circuit of the arithmetic unit is shown in Figure 2.1. Two 4-bit 74LS181 forms an 8-bit word length ALU. Two 8-bit 74LS273 are used as working registers DR1 and DR2 to temporarily store the operands involved in the operation. The data participating in the operation is sent to the working register through the three state gate 74LS245 through the data switch, and the operation result of the ALU is also sent to the data display light through the three state gate 74LS245.

The operands involved in the operation are set by 8 binary switches from SW7 to SW0. When SW-BUS=0, the data is output to DR1 and DR2 through the tractate gate 74LS245. DR1 is connected to the A input port of ALU, and DR2 is connected to the B input port of ALU. Input data into DR1 on the rising edge of P1 and send it to input port A of 74LS181; Input data into DR2 on the rising edge of P2 and send it to input port B of 74LS181.

ALU consists of two pieces of 74LS181, where 74LS181 (1) performs low 4-bit arithmetic logic operations and 74LS181 (2) performs high 4-bit arithmetic logic operations. The carry output signal Cn+4 of 74LS181 (1) is connected to the carry input signal Cn of 74LS181 (2), and the control signals S3~S0, M of the two pieces of 74LS181 are connected respectively. The calculation result is output to the data display light through a three state gate 74LS245. In addition, the carry output signal Cn+4 of 74LS181 (2) can be connected to another indicator light for display carry flag signal status.

# Experimental content and steps

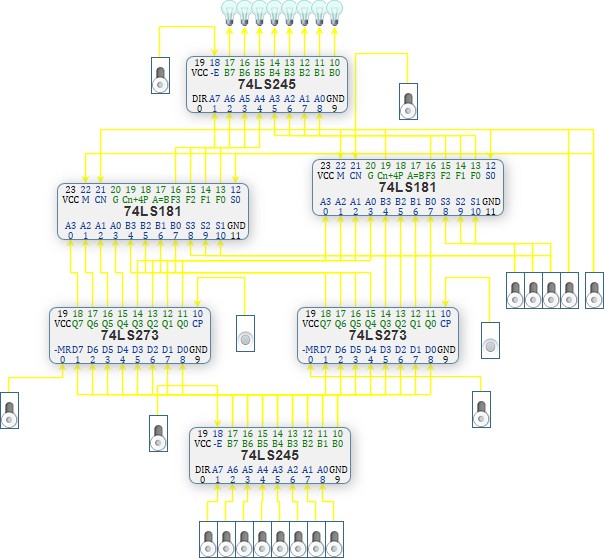


Figure 2.2 Virtual experimental circuit of arithmetic unit

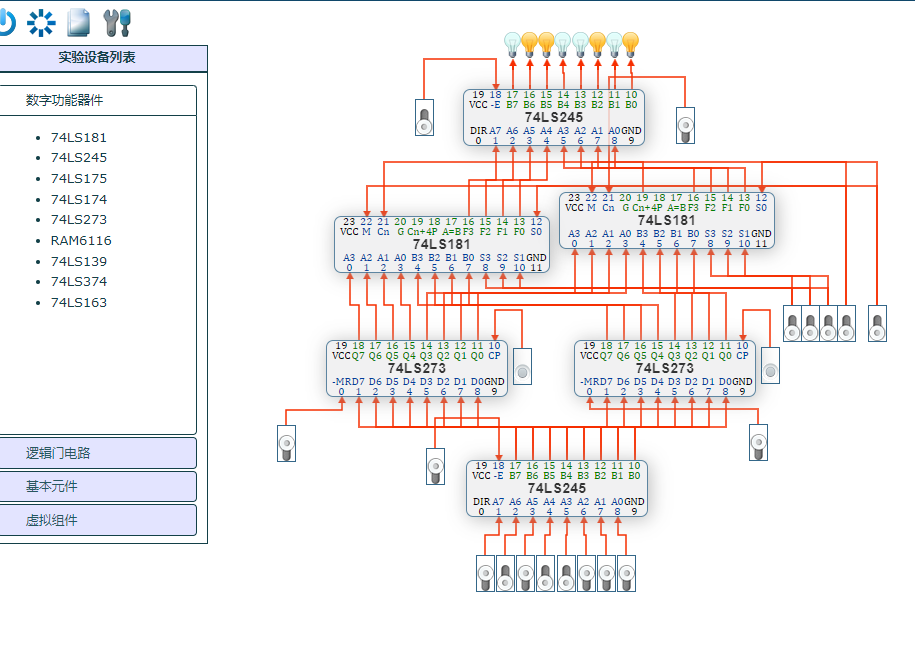
1. Run the virtual experimental system, draw the experimental circuit of the arithmetic unit according to Figure 2.1, and generate the experimental circuit as shown in Figure 2.2:
2. Perform circuit presetting, the specific steps are as follows:
   1. Set ALU-BUS to high level and close the tractate gate of the ALU output terminal;
   2. Set both MR of 74LS273 to high level, otherwise 74LS273 will remain in a reset state.
3. Turn on the power switch.
4. Set the number of SW7~SW0 to DR1 and DR2. Taking DR1=65H and DR2=A7H as an example, the specific steps are as follows:
   1. Set SW-BUS to 0 and open the three state gate at the data input end;
   2. Set SW7~SW0 of the data switch to 01100101;
   3. Send a P1 single pulse signal, and at the rising edge of P1, input the data into register DR1;
   4. Set the SW7~SW0 of the data switch to 10100111;
   5. Send a P2 single pulse signal, and at the rising edge of P2, the data is entered into register DR2.
   6. Set SW-BUS to 1 and close the three state gate at the data input end;
5. Verify if the numbers stored in DR1 and DR2 are correct. The specific operation is as follows:
   1. ALU − BUS=0, open the tractate gate at the ALU output end;
   2. Set Cn=1, ALU has no carry input;
   3. Set S3, S2, S1, S0, and M to 00000, and the indicator light should display data 01100101 in DR1;
   4. Set S3, S2, S1, S0, and M to 10101, and the indicator light should display data 10100111 in DR2.
6. Verify the arithmetic and logical operation functions of 74LS181 (using positive logic). Given DR1=65H and DR2=A7H, change the functional mode of the solver, observe the output of the solver, fill in Table 2-1, and compare and verify with the theoretical values.

**Table 2-1 Validation of Arithmetic Functions**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Work mode selection  S3 S2 S1 S0 | Arithmetic operation (M=0) (Cn=1 without carry) | | | | Logical operation (M=1) | | | |
| function | | Output value | | function | | Output value | |
| 0000 | | Screenshot 2024-05-11 at 5.14.31 PM | | 01100101 | | Screenshot 2024-05-11 at 5.16.25 PM | | 10011010 |
| 0001 | | 11100111 | | 00011000 |
| 0010 | | 01111101 | | 10000010 |
| 0011 | | 11111111 | | 00000000 |
| 0100 | | 10100101 | | 11011010 |
| 0101 | | 00100111 | | 01011000 |
| 0110 | | 10111101 | | 11000010 |
| 0111 | | 00111111 | | 01000000 |
| 1000 | | 10001010 | | 10111111 |
| 1001 | | 00001100 | | 00111101 |
| 1010 | | 10100010 | | 10100111 |
| 1011 | | 00100100 | | 00100101 |
| 1100 | | 11001010 | | 11111111 |
| 1101 | | 01001100 | | 01111101 |
| 1110 | | 11100010 | | 11100111 |
| 1111 | | 01100100 | | 01100101 |

Note: A and B represent the two numbers involved in the operation, "+" represents logical OR, and "plus" represents arithmetic sum.

**Some Pictures of this Circuit Output:**



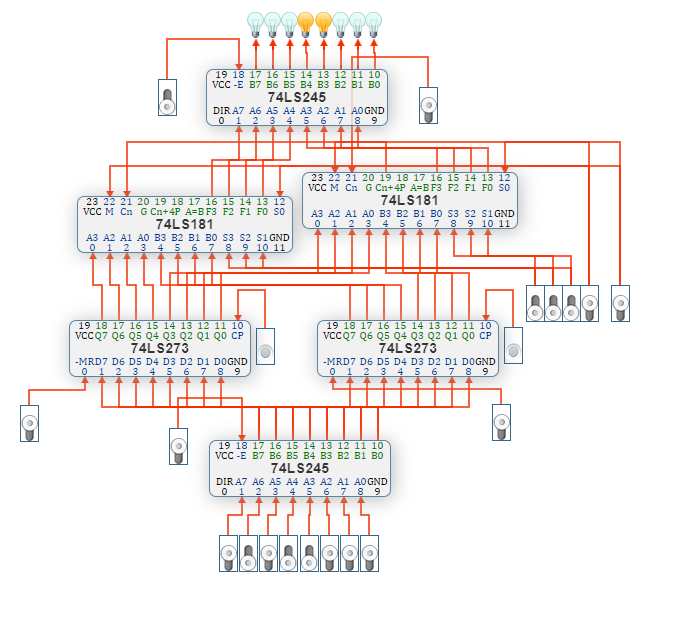
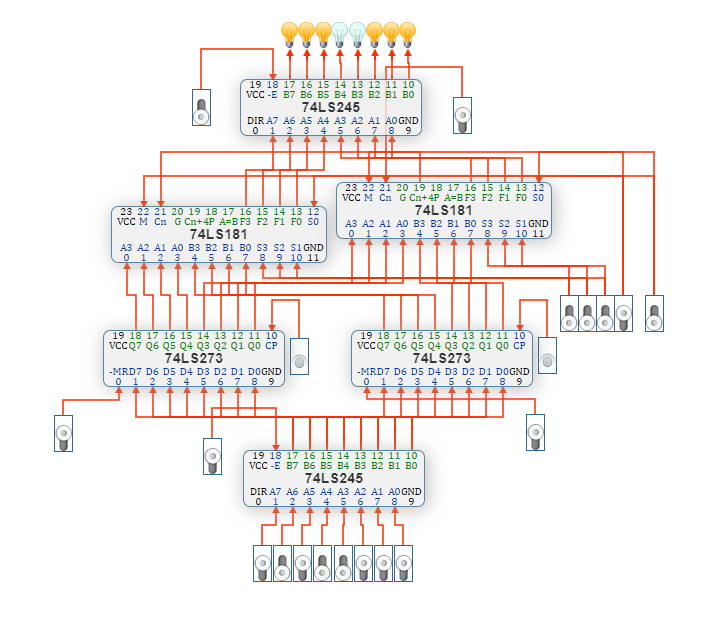
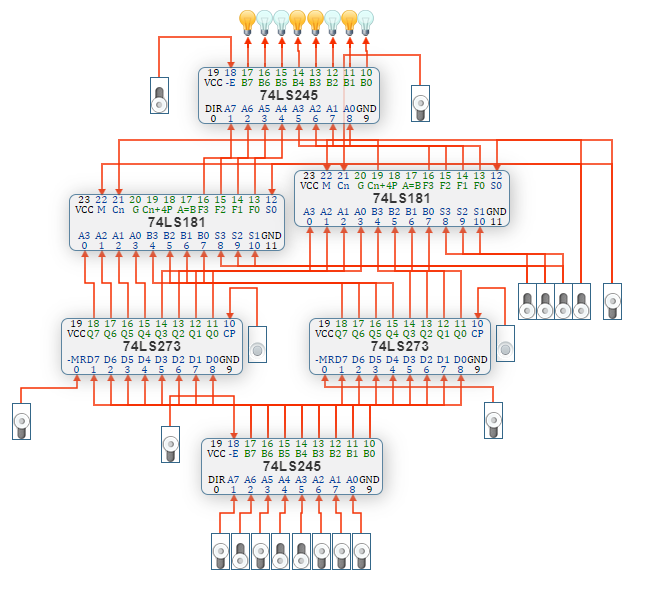


Figure: Circuit diagram and Output

**Validation of Arithmetic and Logical Operations of the 74LS181 ALU**

**Objective**

The objective of this validation is to verify the correct operation of the 74LS181 Arithmetic Logic Unit (ALU) in performing arithmetic and logical functions. The ALU is configured to operate in positive logic mode and is tested with two 4-bit binary numbers, A and B, represented by hexadecimal values DR1=65H and DR2=A7H, respectively.